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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/993,704 | 11/27/2001 | Haruyasu Okubo | HITA.0127 | 8383 |

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| EXAMINER | |
|---|---|
| YANCHUS III, PAUL B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/993,704 | OKUBO ET AL. | |
| | Examiner | Art Unit | |
| | Paul B. Yanchus | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-13 and 15-26* is/are rejected.

7)☒ Claim(s) *7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This final office action is in response to amendments filed on 4/7/05.

### *Claim Objections*

Claim 26 is objected to because of the following informalities: The phrase "can access" seems to be erroneously added in line 8 of claim 26. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ober, US Patent no. 6,665,802, in view of, Applicant's Admitted Prior Art [AAPA].

Regarding claims 1 and 10, Ober discloses a data processor, comprising:

a central processing unit which is capable of executing an instruction [core CPU];

a clock pulse generator that enables frequency multiplication and frequency division operation to a clock signal and is capable of outputting a plurality of clock signals [clock subsystem, column 8, lines 53-64];

other circuit modules [selected peripheral subsystems that do not receive clocks in the sleep mode (clock distributed mode), column 15, lines 39-67]; and

wherein the data processor has a plurality of operation modes including a standby mode, a light standby mode, sleep mode and a program running mode, wherein in the program running mode, the central processing unit is capable of executing instructions [RUN in Table 8 in column 12],

wherein in the sleep mode [IDLE MODE], the clock pulse generator operates the frequency multiplication and frequency division operation, stops supplying one of the clock signals to the central processing unit is stopped and supplies the remaining clock signals to the other circuit modules [column 15, lines 15-21];

in the standby mode [SLEEP MODE], the clock pulse generator is made to stop operating, and to stop supplying the clock signals to the central processing unit and other circuit modules [PLL is shutdown and clocks are removed from the core CPU and selected peripheral subsystems, column 16, lines 9-16]; and

in the light standby mode [SLEEP MODE (clock distributed mode)], the clock pulse generator operates the frequency multiplication and frequency division operation and stops supplying the clock signals to the central processing unit and other circuit modules [clocks are stopped for the CPU and selected peripheral subsystems, but PLL is not stopped to achieve power savings with a quick response to interrupt wake events, column 15, lines lines 39-67].

Ober does not explicitly disclose a frequency multiplication operation in the clock pulse generator. However, Ober does disclose a PLL circuit in the clock pulse generator. AAPA states that it is well known in the art that PLL circuits are used for frequency multiplication operations [page 1, paragraph 2]. Therefore, it would have been obvious o one of ordinary skill in the art to use the PLL in the Ober system to perform a frequency multiplication operation.

Regarding claims 2 and 11, Ober discloses a mode control circuit [power management subsystems] that sets the system power modes based on the state of control registers [power management state machine, column 5, lines 59-62] when a predetermined instruction is executed by the central processing unit [power modes are entered under program control, column 15, lines 43-44 and column 16, lines 9-11].

Regarding claim 3, Ober discloses resetting the sleep mode in response to an external interrupt request and moving the central processing unit to an executable state [column 15, lines 29-30].

Regarding claim 4, Ober discloses resetting the light standby mode in response to an external interrupt request and moving the central processing unit to an executable state [column 15, lines 64-66].

Regarding claim 5, Ober discloses resetting the standby mode in response to an external interrupt request and moving the central processing unit to an executable state [column 16, lines 16-18].

Regarding claim 8, Ober discloses that the mode control circuit stops the supply of a synchronizing clock by causing the processor to halt execution [column 15, lines 25-27].

Regarding claim 9, Ober discloses that the mode control circuit stops the output of the synchronizing signals to the central processing unit and the other circuits [column 15, lines 46-48].

Claims 6, 12, 13 and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ober, US Patent no. 6,665,802, and Applicant's Admitted Prior Art [AAPA], in view of, Sakai, US Patent no. 6,266,776.

Regarding claim 6, Ober teaches that the other circuits may be system timers, but does not explicitly state the system timers are used to determine when to change power modes. However, as disclosed by Sakai using timers to count up to a predetermined value is a well known method used to determine when to change power modes. Therefore, it would have been obvious to one of ordinary skill in the art to use timers to count up to a predetermined value as a means for determining when to change power modes.

Regarding claims 12, 13 and 22, Ober discloses a data processor, comprising:

a central processing unit which is capable of executing an instruction [core CPU];

a clock pulse generator that enables frequency multiplication and frequency division operation on an input clock and outputs a plurality of clock signals [clock subsystem, column 8, lines 53-64];

other circuit modules [selected peripheral subsystems that do not receive clocks in the sleep mode (clock distributed mode), column 15, lines 39-67]; and

a mode control circuit [power management subsystem] that controls settings of first and second modes in said other circuit modules [column 5, lines 59-62],

wherein the data processor has a program running mode, a first mode and a second mode,

wherein in the program running mode [RUN], the CPU is capable of executing the instruction;

wherein in the first mode [IDLE MODE], the clock pulse generator is stopped to supply the clock signals to the central processing unit and the clock pulse generator supplies the clock signals to the other circuit modules [column 15, lines 15-21]; and

wherein in the second mode [SLEEP MODE], the clock pulse generator operates the frequency multiplication and frequency division operation and the clock pulse gernerator stops supplying the clock signals to the central processing unit and said other circuit modules [PLL is shutdown and clocks are removed from the core CPU and selected peripheral subsystems, column 16, lines 9-16].

Ober does not explicitly disclose a frequency multiplication operation in the clock pulse generator. However, Ober does disclose a PLL circuit in the clock pulse generator. AAPA states that it is well known in the art that PLL circuits are used for frequency multiplication operations [page 1, paragraph 2]. Therefore, it would have been obvious to one of ordinary skill in the art to use the PLL in the Ober system to perform a frequency multiplication operation.

Ober teaches that the other circuits may be system timers, but does not explicitly state the system timers are used to determine when to change power modes. However, as disclosed by Sakai, using timers to count up to a predetermined value is a well known method used to determine when to change power modes. Therefore, it would have been obvious to one of ordinary skill in the art to use timers to count up to a predetermined value as a means for determining when to change power modes.

Regarding claims 15 and 23, Ober discloses a mode control circuit [power management subsystems] that sets the system power modes based on the state of control registers [power management state machine, column 5, lines 59-62] when a predetermined instruction is executed

by the central processing unit [power modes are entered under program control, column 15, lines 43-44 and column 16, lines 9-11].

Regarding claim 16, Ober discloses resetting the first mode in response to an external interrupt request and moving the central processing unit to an executable state [column 15, lines 29-30].

Regarding claim 17, Ober discloses resetting the second mode in response to an external interrupt request and moving the central processing unit to an executable state [column 16, lines 16-18].

Regarding claim 18, Ober discloses that the mode control circuit stops the supply of a synchronizing clock by causing the processor to halt execution [column 15, lines 25-27].

Regarding claims 19-21, Ober discloses that the mode control circuit stops the output of the synchronizing signals to the central processing unit and the other circuit modules [column 15, lines 46-48].

Regarding claims 24 and 26, Ober discloses a memory that the central processing unit can access [column 5, lines 50-52] and a circuit that requests an interrupt from the data processor [column 5, lines 53-55].

Regarding claim 25, Ober discloses that the system is a battery-powered device [column 1, lines 23-25].

***Allowable Subject Matter***

Claims 7 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

Applicant's arguments filed on 4/7/05 have been fully considered but they are not persuasive.

Regarding claim 1 and 12, Applicant argues that the cited prior art references do not teach or suggest "a light standby mode (claim 1) or a second power mode (claim 12) in which the clock pulse generator operates the frequency multiplication and frequency division operation, but stops supplying clock signals to a CPU and other circuit modules." The examiner disagrees. Ober discloses a power mode [sleep mode (clock distributed mode)] in which a clock generator operates, but stops supplying clocks to the CPU and other circuit modules [column 15, lines 39-57]. Ober discloses selecting which peripherals receive clocks during the sleep mode and which peripherals do not receive clocks during the sleep mode using SFR registers [column 3, lines 60-67 and column 4, lines 16-28]. The examiner interprets "other circuit modules" to be the selected peripherals that do not receive clocks during the sleep mode. AAPA is relied upon to teach that frequency multiplication circuitry is a well known part of PLL clock generating circuits [page 1, paragraph 2]. Therefore, the cited prior art references do teach, "a light standby mode (claim 1) or a second power mode (claim 12) in which the clock pulse generator operates the frequency multiplication and frequency division operation, but stops supplying clock signals to a CPU and other circuit modules."

The rejections to claims 1-6, 8-13 and 15-26 are respectfully maintained.

*Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
June 27, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100